REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-4 and 6-11 remain in the application. Claims 1 and 10 have been amended. Claims 5 and 12 have been previously cancelled. Method claims 10-11 have been previously withdrawn and rejoinder of claims 10-11 has been requested.

In item 1 on pages 2-4 of the final Office action dated March 25, 2005, claims 1-2, 4, 6, and 8 have been rejected as being unpatentable over Cho (US 6,087,718) in view of Lin et al. (US 6,593,649) under 35 U.S.C. § 103(a).

In item 2 on pages 5-8 of the final Office action dated March 25, 2005, claims 1-4 and 6-9 have been rejected as being unpatentable over Chang et al. (US 6,483,181) in view of Lin et al. under 35 U.S.C. § 103(a).

In item 3 on pages 8-9 of the final Office action dated March 25, 2005, claims 7 and 9 have been rejected as being unpatentable over Cho in view of Lin et al. and further in view of Chang et al. under 35 U.S.C. § 103(a).

The rejections have been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 3, lines 24-26 of the specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> said contact surfaces of said first semiconductor chip and said second semiconductor chip being disposed at mutually congruent positions;
>
> a first interposer layer or interposer film configured on said active surface of said first semiconductor chip, said first interposer layer or interposer film having first bonding fingers, first interposer lines and first bonding surfaces; and
>
> a second interposer layer or interposer film configured on said active surface of said second semiconductor chip, said second interposer layer or interposer film having second bonding fingers, second interposer lines and second bonding surfaces;
>
> each one of said plurality of first bonding connections connecting one of said first bonding surfaces on said first interposer layer or interposer film to said inner section of one of said plurality of flat conductors; and
>
> each one of said plurality of second bonding connections connecting one of said second bonding surfaces on said second interposer layer or interposer film to said transitional section of one of said plurality of flat conductors.

The invention of the instant application has the object of providing an electronic component having stacked semiconductor chips in which the contact surfaces of each of the chips are arranged at mutually congruent positions. This technical construction is of particular relevance in providing electronic components with a higher memory density since it is desired to stack substantially identical semiconductor memory chips in the same package. The memory capacity of the component can, therefore, be doubled by stacking two memory chips in the package.

Neither Cho nor Lin et al. have the above-mentioned object, nor provide any teaching which would lead a person skilled in the art to the semiconductor component according to amended independent claim 1 of the instant application.

Cho fails to teach a stacked electronic component in which the contact surfaces of the first and second semiconductor chips are arranged at mutually congruent positions. Cho teaches a package, as can be seen in Fig. 2, in which the lower semiconductor chip 5 includes contact areas 4 disposed in the lateral center of the active surface. In contrast, the upper semiconductor chip 7 includes contact areas 6 disposed at the peripheral edges of the active surface.

Cho also fails to teach semiconductor chips with an interposer film and, consequently, also fails to teach a component including first bonding connections between an interposer layer or interposer film and the inner section of a flat conductor and second bonding connections between an interposer film or layer and the transitional section of a flat conductor.

The Examiner has stated in the Response to Arguments on page 2 of the Advisory action dated May 17, 2005 that Lin et al. teach that, by providing an interposer on the active surface of the chip, this would allow the input/output pads location for the packaging of semiconductor devices of different dimensions using a universal package. Furthermore, the Examiner has stated that Lin et al. teach that the interposer enables easy connection between the I/O pads and the different format packages.

Therefore, Lin et al. teach mounting single chips of different dimensions in the same type of package. In contrast, the invention of the instant application addresses the problem of stacking two chips with mutually congruent contact areas in a package.

Lin et al. fail to teach an electronic component, which includes two stacked semiconductor chips. Lin et al. fail to address the problem of stacking semiconductor chips in a package and thus fail to provide the structure of stacking semiconductor chips in which the contact surfaces on the active surfaces of the semiconductor chips are arranged at mutually congruent positions.

The teaching of Lin et al. relates to a totally different technical problem. Applicants, therefore, maintain the view that a person skilled in the art would not look to Lin et al. when looking to solve the technical problem addressed by the invention of the instant application. Even if a person skilled in the art did look to Lin et al., the component according to claim 1 of the instant application is not obvious.

Lin et al. fail to provide any indication that the provision of an interposer layer or interposer film on each of two semiconductor chips in a stack solve the problem addressed by the invention of the instant application. Lin et al. fail to provide a teaching that this structure would enable two semiconductor chips, in which the contact areas on each semiconductor chip are arranged at mutually congruent positions, to be stacked in an electronic component so that

the component includes a first plurality of bonding connections between the first interposer film and the inner section of a flat conductor in addition to a second plurality of bonding connections stretching between the second interposer and the transitional section of the flat conductor.

The other cited references do not make up for the deficiencies of Cho and Lin et al.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-4 and 6-9 are solicited. Rejoinder of method claims 10-11 is requested upon allowance of the product claims under MPEP 821.04 ("if applicant elects claims directed to the product, and a product claim is subsequently found allowable, withdrawn process claims which depend from or otherwise include all the limitations of the allowable product claim will be rejoined").

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Yonghong Chen
Reg. No. 56,150

For Applicants

YC

June 27, 2005

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101